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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,542	10/23/2003	Takefumi Endo	H-1118	6429

7590 06/17/2005

Mattingly, Stanger & Malur, P.C.
Suite 370
1800 Diagonal Road
Alexandria, VA 22314

EXAMINER	
MIS, DAVID C	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/690,542	ENDO, TAKEFUMI	
	Examiner	Art Unit	
	David Mis	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *9 and 10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1023*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 4, 5, 7 and 8 are rejected under 35 U.S.C. 102(a.) as being clearly anticipated by Asikainen et al.

Asikainen et al disclosed a semiconductor integrated circuit (column 3, lines 48-52) comprising an oscillation circuit having inductance and capacitance (Figure 2) and a frequency dependent on LC (column 4, lines 9-56) and a voltage comparing circuit comparing the VCO control voltage with a reference voltage (Figure 3, column 6, lines 36-42) wherein the oscillator has a plurality of capacitance elements connected in parallel and a selection switch means (Figure 2, column 4, lines 28-33) and can change LC values by selectively connecting any one of the plural capacitance elements with the selection switch means (Figure 2, column 4, lines 26-28) and the selection switch means is controlled depending on the comparison result of the voltage comparing circuit to adjust the oscillation frequency of the oscillation circuit (Figure 3, column 6, line 56 to column 7, line 38); the capacitance elements having binary weights (column 4, lines 33-41); including a register for sequentially storing the comparison result of the

voltage comparing circuit, each bit controlling the selection switch means (Figure 3, counter register having bits N1, ..., Nn, column 6, lines 7-11); transmission control means (11, 15) between the voltage comparing circuit (12) and the register (13), (Figure 3), which transfers or cuts off the output of the voltage comparing circuit (column 6, line 25 to column 7, line 38) and is set to become conductive when the power source voltage rises (once the circuit is powered, the digital value output from comparator 12 is conducted through AND gates 11 and 15 depending on the control levels on the other AND gate inputs) and controls register (13) to sequentially store the comparison result (timed by timer 10 and stored as the result of counting, column 5, lines 41-58) and is usually in the cut-off condition during normal oscillation operation (column 6, lines 12-24).

3. Claims 3 and 6 are rejected under 35 U.S.C. 102(a.) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Asikainen et al.

Asikainen et al disclosed that which is claimed as described above and disclosed that the capacitance sizes were weighted as described above; and varying the size of capacitances in integrated circuits was done by forming plate areas of appropriate sizes, which plate areas when large were the same as parallel connected smaller plate areas and for such capacitances it

was known to use combinations of identical smaller capacitors to form the larger ones and although Asikainen et al did not say how they formed their capacitances, it is presumed that this type of sizing methodology is covered by their disclosure since there is no reason to presume that it is not or that another one would be exclusively. It would have been obvious to one of ordinary skill in the art to have incorporated parallel identical capacitors to form larger capacitances in the Asikainen et al circuit and "motivated" as taught in the integrated circuit forming art that encompasses the integrated circuit oscillator art. For example, see O'Shaughnessy Figure 8B-1.

4. Applicant's election without traverse of Group I, claims 1-8, in the reply filed on 06/02/05 is acknowledged.

Claims 9 and 10 are withdrawn from consideration as not directed to the elected Group.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Mis whose telephone number is (571) 272-1765. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Mis
Primary Examiner
Art Unit 2817